CLAIMS

What is claimed is:

1. A field effect transistor comprising:

a substrate having source and drain regions;

a gate insulator above said substrate;

a notch-shaped gate conductor above said gate insulator, said notch-shaped gate conductor comprising at least two layered sections, including an upper layer and a lower layer,

wherein said layered sections comprise at least two different materials, one of which comprises silicon-germanium, and

wherein said lower layer has a higher etch rate than said upper layer.

2. The field effect transistor according to claim 1, wherein said upper layer comprises polysilicon-germanium and said lower layer is selected from a group consisting of amorphous silicon and polysilicon.

3. The field effect transistor in claim 2, wherein said amorphous silicon and polysilicon are devoid of germanium.

4. The field effect transistor according to claim 1, wherein said lower layer and said upper layer comprise polysilicon-germanium (poly-SiGe) having concentrations of germanium that increase along a depth of said upper layer section and said lower layer section.

5. The field effect transistor according to claim 4, wherein an increase in said concentrations of germanium is directly proportional to a depth between a bottom of said lower layer and a top of said upper layer.

6. The field effect transistor in claim 1, wherein said upper layer and said lower layer comprise materials capable of being simultaneously etched.

7. A field effect transistor comprising:

a substrate having source and drain regions;

a gate insulator above said substrate;

a notch-shaped gate conductor above said gate insulator, said notch-shaped gate conductor comprising at least two layered sections, including an upper layer and a lower layer,

wherein said upper layer comprises polysilicon and said lower layer comprises amorphous silicon, and

wherein said lower layer has a higher etch rate than said upper layer.

8. The field effect transistor according to claim 7, wherein said upper layer section comprises polysilicon-germanium.

9. The field effect transistor in claim 8, wherein said amorphous silicon is devoid of germanium.

10. The field effect transistor in claim 7, wherein said upper layer and said lower layer comprise materials capable of being simultaneously etched.

11. A method for making a field effect transistor having a notch-shaped gate conductor, said method comprising:

forming a gate insulator above a substrate;

depositing a gate conductor material over said gate insulator, wherein said gate conductor material comprises at least two layered sections, including an upper layer and a lower layer, said layered sections comprising at least two different materials, one of which comprises silicon-germanium, and said lower layer having a higher etch rate than said upper layer;

etching said gate conductor material through a mask to define a notch-shaped gate conductor;

doping said notch-shaped gate conductor and said substrate, to make said notch-shaped gate conductor conductive, and to form source and drain regions in said substrate.

12. The method in claim 11, wherein said upper layer comprises polysilicon-germanium and said lower layer is selected from a group consisting of amorphous silicon and polysilicon.

13. The method in claim 12, wherein said amorphous silicon and polysilicon are devoid of germanium.

14. The method in claim 11, wherein said lower layer and said upper layer comprise polysilicon-germanium (poly-SiGe) having concentrations of germanium that increase along a depth of said upper layer section and said lower layer section.

15. The method in claim 14, wherein an increase in said concentrations of germanium is directly proportional to a depth between a bottom of said lower layer and a top of said upper layer.

16. The method in claim 11, wherein said etching of said gate conductor material comprises a single etching process.

17. A method for making a field effect transistor having a notch-shaped gate conductor, said method comprising:

forming a gate insulator above a substrate;

depositing a gate conductor material over said gate insulator, wherein said gate conductor material comprises at least two layered sections, including an upper layer and a lower layer, said upper layer comprising polysilicon, said lower layer comprising amorphous silicon, and said lower layer having a higher etch rate than said upper layer;

etching said gate conductor material through a mask to define a notch-shaped gate conductor; and

doping said notch-shaped gate conductor and said substrate, to make said notch-shaped gate conductor conductive, and to form source and drain regions in said substrate.

18. The method in claim 17, wherein said upper layer section comprises polysilicon-germanium.

19. The method in claim 18, wherein said amorphous silicon is devoid of germanium.

20. The method in claim 17, wherein said etching of said gate conductor material comprises a single etching process.